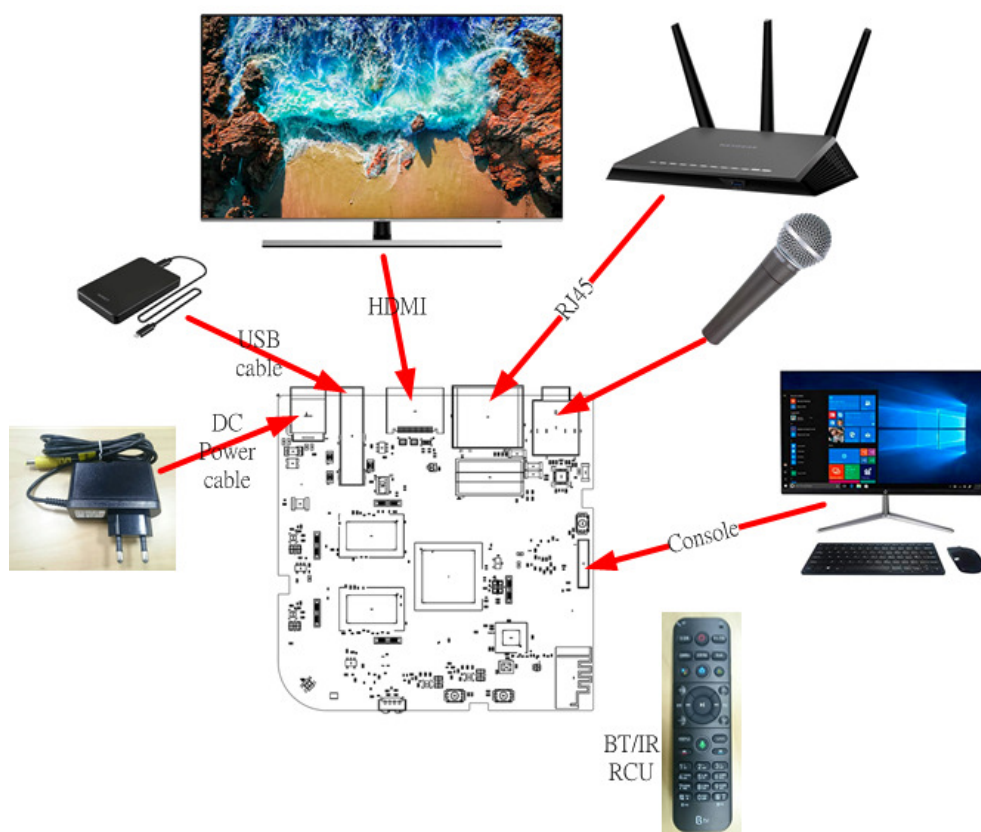


Hardware Unit Test Report

Power Consumption Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
V005	4.9.113 #1MonFeb 1122:40:43 CST 2019	S/N:	KLM8G1GETF-B041

1. Power Test Setup



2. Test Command

ADC function command:

ADC for MIC function is required by command as below:

```
tinycap /data/test.wav -D 0 -d 1 -r 48000
```

eMMC function command:

Because of playing 4K HDR video from Smart YouTube, the eMMC function does not read or write. We can use command to do read/write eMMC function while playing 4K HDR video on Smart YouTube through console. The command is as below:

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eMMC Read/Write Test command

(1)write 1G

```
time sh -c "dd if=/dev/zero of=/data/tmp.dd bs=1000k count=1000; sync"
```

(2)read 1G

```
time sh -c "dd if=/dev/block/data of=/dev/zero bs=1000k count=1000; sync"
```

(3)read 8G

```
time sh -c "dd if=/dev/block/data of=/dev/zero bs=1000k count=8000; sync"
```

3. Test Condition

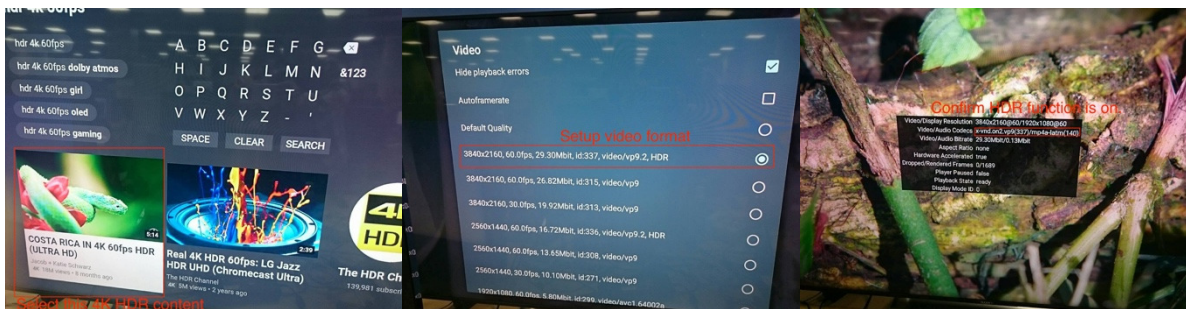
Ethernet: 1Gb.

BOX plays 4Kp60HDR video from Smart YouTube.

USB port: Mounted 2.5 inch USB HDD.

BT RCU: connected.

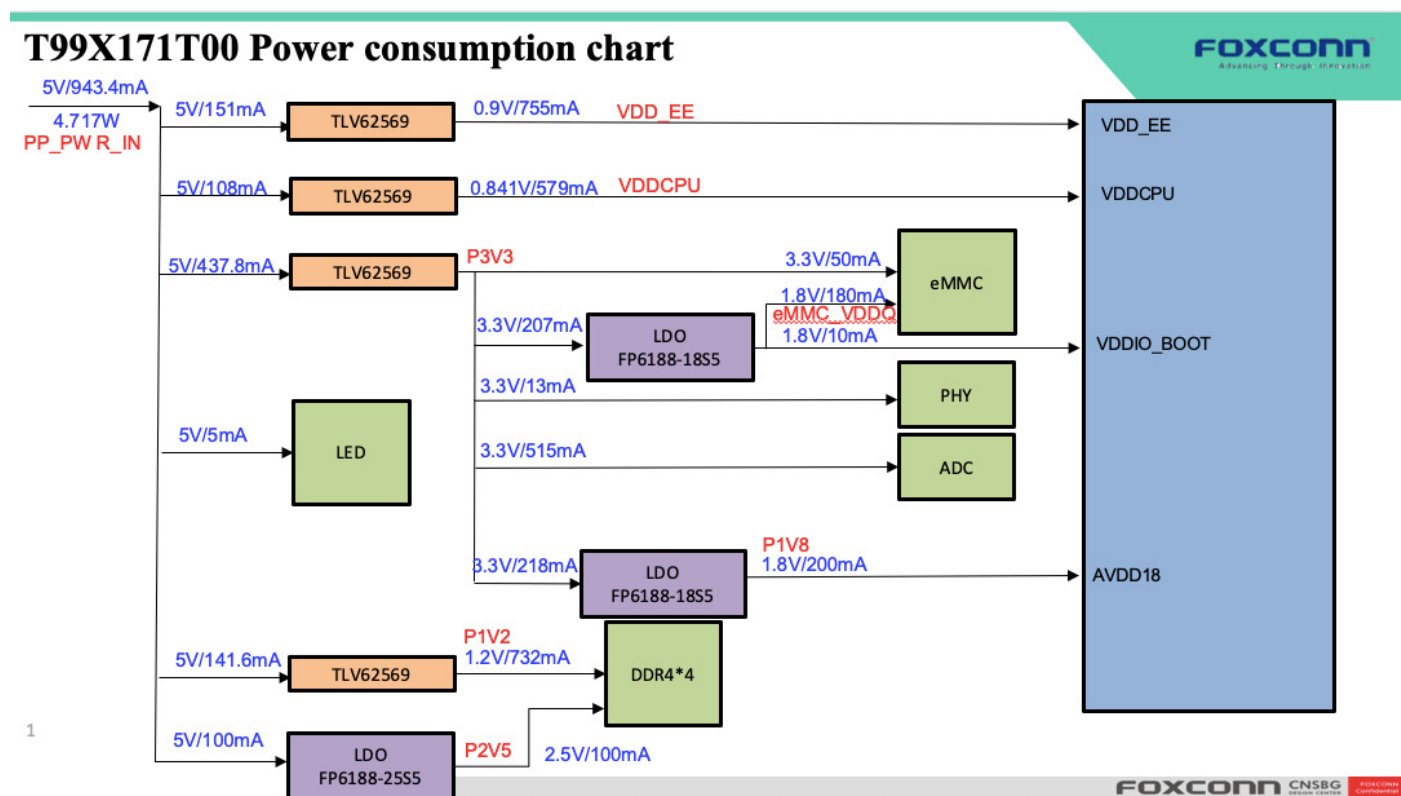
Playing video: COSTA RICA IN 4K 60fps HDR(ULTRA HD), see below example pictures.



For USB HDD issue, while testing, the USB HDD is plugged first then plugged-in power final. The boot is ok. The mean value of DC power instantly is 5.1W while plugging DC power cable onto DC jack. The test repeats are 10 times, the boot test with USB HDD is ok to boot up.

Plugged-in and plugged-out USB HDD repeats for 10 times, the Eagle board is ok and does not cause re-boot.

4. Power Architecture



5. Result and Picture

Power Rail	Power IC / MOSFET P/N	Power IC / MOS	Measurement point	Result (A)	Picture
PP_PWR_IN	BSY012U050200U 5V/2A	2A	F301	1008mA	Fig. 1
VDD_EE	TLV62569DRLR	2A	L302	688.8mA	Fig. 2
VDDCPU	TLV62569DRLR	2A	L301	368.5mA	Fig. 3
P1V2	TLV62569DRLR	2A	L303	553.4mA	Fig. 4
P3V3	TLV62569DRLR	2A	L304	280.5mA	Fig. 5
eMMC_VDDQ	FP6188-18S5	600mA	R606	83.74mA	Fig. 6
P1V8	FP6188-18S5	600mA	R324	77.61mA	Fig. 7
P2V5	FP6188-25S5	600mA	R325	7.988mA	Fig. 8

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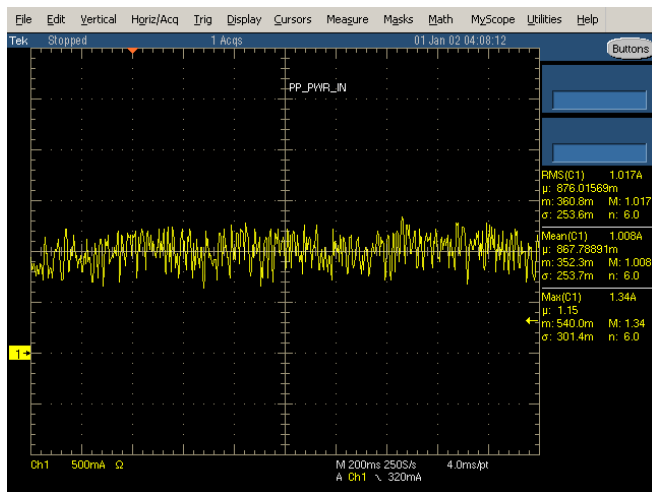


Fig. 1: PP_PWR_IN

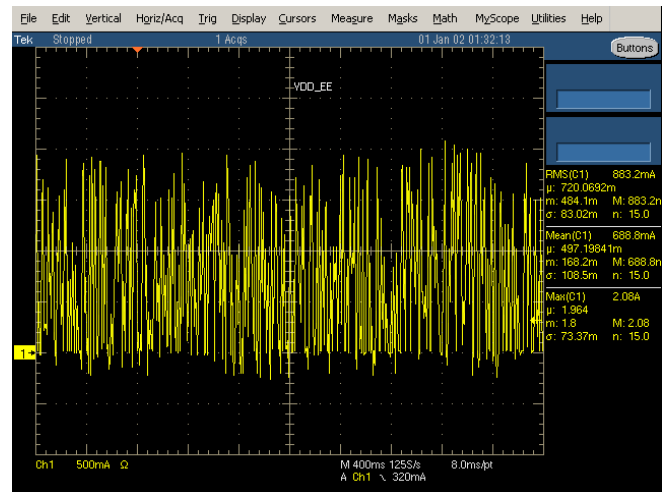


Fig. 2: VDD_EE

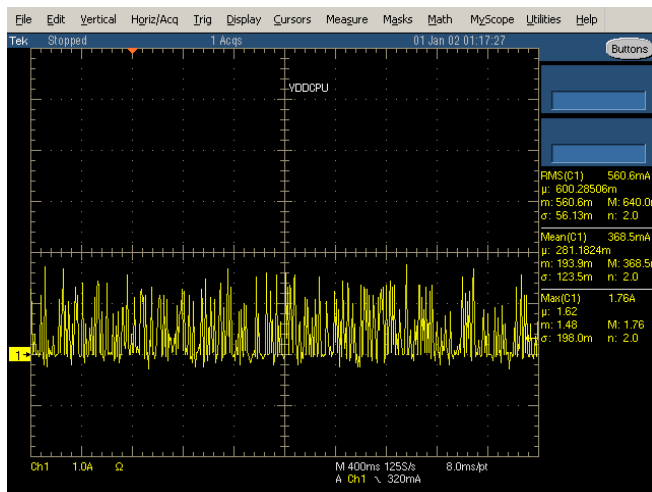


Fig. 3: VDDCPU

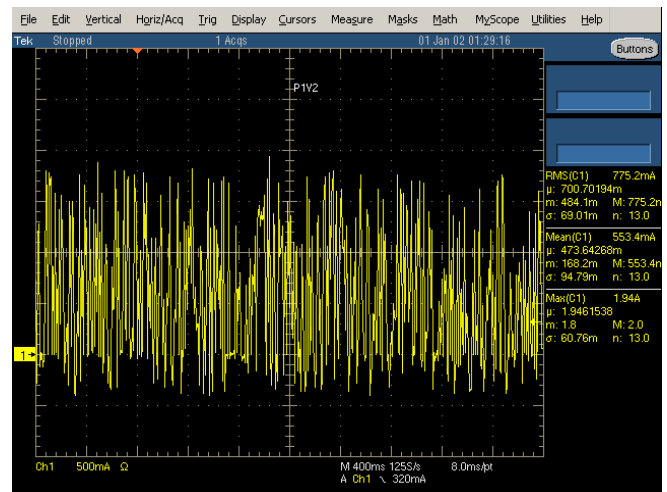


Fig. 4: P1V2

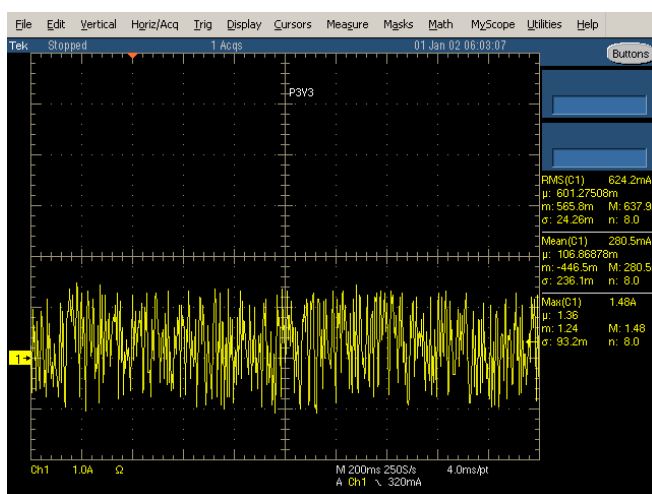


Fig. 5: P3V3

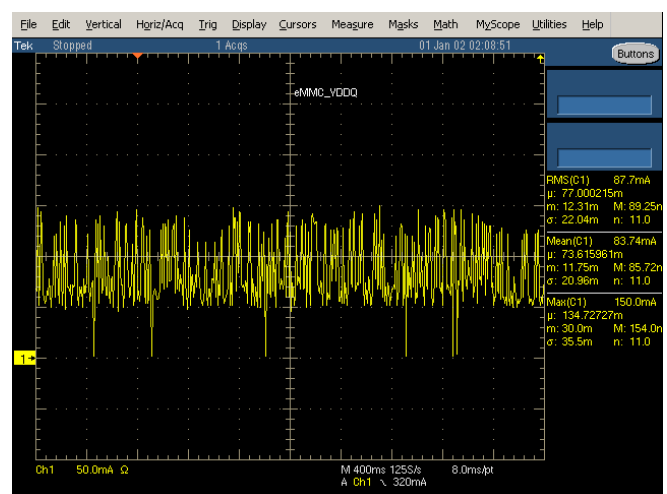


Fig. 6: eMMC_VDDQ

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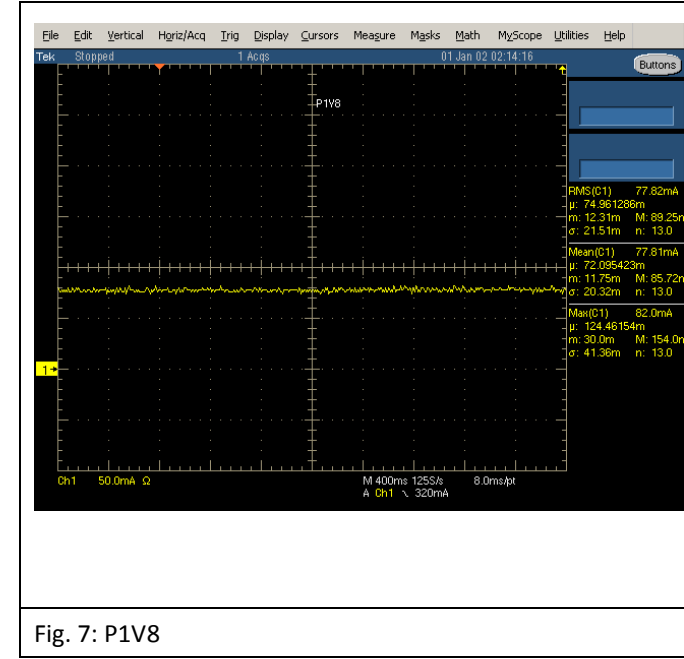


Fig. 7: P1V8

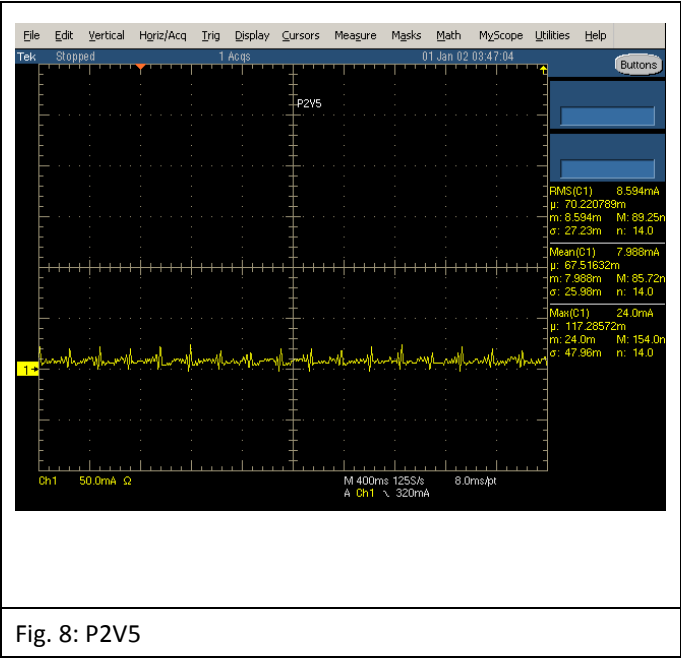


Fig. 8: P2V5